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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,836	04/04/2001	Kazunori Shionoya	018656-232	1177

7590 08/09/2006

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EXAMINER	
MILIA, MARK R	

ART UNIT	PAPER NUMBER
2625	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,836	SHIONOYA, KAZUNORI	
	Examiner	Art Unit	
	Mark R. Milia	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment was received on 5/24/06 and has been entered and made of record. Currently, claims 1-14 are pending.

Response to Arguments

2. Applicant's arguments filed 5/24/06 have been fully considered but they are not persuasive.

The applicant asserts, on pages 5-7, that the reference of Kumakura does not disclose a printed circuit board with mounted memory modules and a mounted memory controller and connectors for enabling the printed circuit board to be attached to an apparatus. The examiner respectfully disagrees as Kumakura does disclose such a feature. Particularly, Kumakura shows in Figs. 4 and 5 a printed circuit board with mounted memory modules and connector terminals. Further, Kumakura states in column 6 lines 65-67 that a memory controller can also be mounted to the printed circuit board. The applicant also asserts that the combination of Ho and Kumakura does not teach or suggest a memory board having a memory device and a memory controller mounted directly thereon which is adapted to be connected to another apparatus which utilizes the memory device. The examiner respectfully disagrees as the combination of

Ho and Kumakura does disclose such features. Particularly, as stated above, Kumakura discloses a printed circuit board with mounted memory modules and a mounted memory controller and connectors for enabling the printed circuit board to be attached to an apparatus. Ho discloses a memory system in which memory modules can be inserted into module sockets. Therefore, it would have been obvious to replace the memory module of Ho with the printed circuit board of Kumakura. It is well known in the art to provide detachable memory modules (printed circuit boards with mounted memory chips) that can be used with a plurality of apparatuses.

Therefore, the rejection of claims 1-14, as cited in the previous Office Action, is maintained and repeated in this Office Action.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (US 5535368) in view of Kumakura et al. (US 6114751).

Regarding claim 1, Ho discloses a memory board comprising a printed wiring board having a connector terminal (see column 1 lines 19-23 and column 3 lines 10-20), a memory device mounted on the printed wiring board and storing data used by an apparatus to which the printed wiring board is to be attached (see column 3 lines 29-34 and 54-64), and a memory controller for converting a control signal from the apparatus

into a control signal suitable for access method specific to the memory device (see column 3 lines 47-51).

Ho does not disclose expressly a memory device mounted on the printed wiring board adapted to be attached by the connector terminal and a memory controller mounted directly on the printing wiring board.

Kumakura discloses a printed wiring board having a connector terminal (see Figs. 4 and 5), a memory device mounted on the printed wiring board adapted to be attached by the connector terminal (see Figs. 4 and 5 and column 6 lines 36-67), and a memory controller mounted directly on the printing wiring board (see Figs. 4 and 5 and column 6 lines 36-67).

Regarding claim 4, Ho discloses an image forming apparatus comprising: a memory board (see column 1 lines 19-23, column 2 lines 15-21, and column 3 lines 10-20), a connector for attaching the memory board (see column 3 lines 29-34), and a controller accessing the attached memory board to perform a control associated with image formation (see column 3 lines 47-50), wherein the memory board, which is connected to the connector, comprises a printed wiring board having a connector terminal, a memory device mounted on the printed wiring board, and storing data used by an apparatus to which the printed wiring board is attached, and a memory controller for converting a control signal from the apparatus into a control signal suitable for access method specific to the memory device (see column 3 lines 40-64, column 4 lines 5-60, and column 5 lines 5-8).

Ho does not disclose expressly a memory device mounted on the printed wiring board adapted to be attached by the connector terminal and a memory controller mounted directly on the printing wiring board.

Kumakura discloses a printed wiring board having a connector terminal (see Figs. 4 and 5), a memory device mounted on the printed wiring board adapted to be attached by the connector terminal (see Figs. 4 and 5 and column 6 lines 36-67), and a memory controller mounted directly on the printing wiring board (see Figs. 4 and 5 and column 6 lines 36-67).

Regarding claim 7, Ho discloses a memory board comprising: a printed wiring board having a connector terminal (see column 1 lines 19-23 and column 3 lines 10-20), a memory device mounted on the printed wiring board, and storing data used by an apparatus to which the printed wiring board is attached (see column 3 lines 29-34 and 54-64), and a memory controller for converting a control signal from the apparatus into a control signal suitable for access method specific to the memory device (see column 3 lines 40-51).

Ho does not disclose expressly a memory device mounted on the printed wiring board adapted to be attached by the connector terminal and a memory controller mounted directly on the printing wiring board.

Kumakura discloses a printed wiring board having a connector terminal (see Figs. 4 and 5), a memory device mounted on the printed wiring board adapted to be attached by the connector terminal (see Figs. 4 and 5 and column 6 lines 36-67), and a

memory controller mounted directly on the printing wiring board (see Figs. 4 and 5 and column 6 lines 36-67).

Ho & Kumakura are combinable because they are from the same field of endeavor, memory devices.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the memory controller mounted directly on the printed wiring board, as described by Kumakura, and which is well known in the art, with the system of Ho.

The suggestion/motivation for doing so would have been to increase processing speed by shortening the distance between memory components.

Therefore, it would have been obvious to combine Kumakura with Ho to obtain the invention as specified in claims 1, 4, and 7.

Regarding claims 2 and 5, Ho and Kumakura disclose the system discussed in claims 1 and 4, and Ho further discloses wherein the memory controller converts a control sent from the apparatus into a control compatible with the kind of the memory device (see column 3 lines 40-51).

Regarding claims 3 and 9, Ho and Kumakura disclose the system discussed in claims 1 and 7, and Ho further discloses wherein the memory controller stores a setting information relevant to the memory device and mediates data communication according to the setting information (see column 3 lines 47-51 and column 4 lines 20-32 and 39-46).

Regarding claim 6, Ho and Kumakura disclose the system discussed in claim 4, and Ho further discloses wherein the memory controller is programmed by the controller of the image forming apparatus (see column 3 lines 40-51).

Regarding claims 8, 13, and 14, Ho and Kumakura disclose the system discussed in claims 1, 4, and 7, and Ho further discloses wherein the memory controller is a programmable device where the content of the conversion is changeable (see column 3 lines 40-50).

Regarding claims 10-12, Ho and Kumakura disclose the system discussed in claims 1, 4, and 7, and Ho further discloses wherein the memory controller is a programmable device (see column 3 lines 40-50).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark R. Milia whose telephone number is (571) 272-7408. The examiner can normally be reached M-F 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler M. Lamb can be reached at (571) 272-7406. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark R. Milia
Examiner
Art Unit 2625

MRM

JOSEPH R. POKRZYWA
PRIMARY EXAMINER